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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,863	02/04/2004	Abdalla Aly Naem	100-19810 (P05402-D01)	6527

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LAW OFFICES OF MARK C. PICKERING
P.O. BOX 300
PETALUMA, CA 94953

EXAMINER	
BREWSTER, WILLIAM M	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/772,863	NAEM ET AL.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *020404*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 10-19, 21, 22, 24, 25, 28, 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Banerjee et al., US Patent No. 6,707,132 B1.

Banerjee anticipates a method of forming a MOS transistor on a semiconductor material of a first conductivity type, the method comprising the steps of:

in fig. 9, forming a layer, or region, of material of the first conductivity type 52 on the semiconductor material 41, the layer of material having silicon, germanium, and carbon, col. 3, lines 49-58;

in fig. 12, forming an insulation layer 65 over the layer of material, col. 3, lines 13-27;

in fig. 13, forming a layer of conductive material on the insulation layer;

etching the layer of conductive material to form a gate; and

forming spaced-apart source and drain regions of a second conductivity type in the layer of material on opposite sides of the gate, unlabelled, col. 4, line 28-36;

limitations from claim 11, the method of claim 10 wherein the forming a layer of

material step includes the step of growing the layer of material on the semiconductor material, col. 3, line 49-58;

limitations from claim 12, the method of claim 10 wherein the forming a layer of material step includes blanket depositing a layer of silicon germanium carbon over the semiconductor material, col. 3, line 59 - col. 4, line 7;

limitations from claim 13, the method of claim 10, in figs. 6-7, wherein an isolation region 43 adjoins the semiconductor material 41, col. 3, lines 49-58; the isolation region having a top surface; and the forming a layer of material step includes the step of selectively epitaxially growing the layer of material on the semiconductor material 52, the layer of material having a top surface that lies below the top surface of the isolation region, col. 3, lines 49-58;

limitations from claim 14, the method of claim 13 wherein the semiconductor material 51 has a bottom surface that is substantially coplanar with the top surface of the isolation region 43, in figs. 10-13;

limitations from claims 15, 28, the method of claims 10, 22 wherein the forming a layer or a region of material step includes the steps of:

in figs. 7-8, removing a portion of the semiconductor material, top portion of 41, to expose an etched surface of the semiconductor material; and

in fig. 9, growing the layer of material 51, 52 on the etched surface of the semiconductor material, col. 3, line 59 - col. 4, line 7;

limitations from claims 16, 29, the method of claims 10, 22 wherein the forming a layer or region of material step includes the steps of:

in figs. 7-8, removing a portion of the semiconductor material to expose an etched surface of the semiconductor material, top layer of 41; and

in fig. 9, blanket depositing a layer of silicon germanium carbon over the etched surface of the semiconductor material, col. 3, line 59 - col. 4, line 7;

limitations from claim 17, the method of claim 12 wherein the forming a layer of material step includes the steps of: in figs. 7-8, removing a portion of the semiconductor material to expose an etched surface of the semiconductor material, top layer of 41, the etched surface of the semiconductor material lying below the top surface of the isolation region; and

epitaxially growing the layer of material on the etched surface of the semiconductor material, col. 3, lines 49-58;

limitations from claim 18, the method of claim 15 and further comprising the step of, in fig. 9, forming a layer of cap silicon 55 on the layer of material prior to the formation of the insulation layer, col. 3, lines 49-58;

limitations from claim 19, the method of claim 10 wherein the layer of material has a substantially uniform concentration of carbon atoms, wherein the alloy is uniform concentration unless otherwise stated, col. 3, lines 49-58;

limitations from claim 22, the method of claim 21 and further comprising a semiconductor material of the first conductivity type, the transistor region 41, the region containing the semiconductor material 51, 52 and lying between the semiconductor material and the insulation layer, col. 3, lines 22-58;

limitations from claim 24, the method of claim 23 wherein the region includes silicon, germanium, and carbon, col. 3, lines 49-58;

limitations from claim 25, the method of claim 22 wherein the region includes silicon, germanium, and carbon, col. 3, lines 49-58.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20, 26, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Banerjee as applied to claims 10-19, 21, 22, 24, 25, 28, 29 above, and further in view of Chu et al., US Publication No. 2002/0182423.

does not specify a non-uniform concentration of carbon in his material, but Chu does. Chu teaches:

limitations from claim 20, the method of claim 10, in fig. 9, line 170, wherein the layer of material, SiGeC, p. 3, ¶ 37, has a non-uniform concentration of carbon atoms, and includes a surface region of a heavy concentration of carbon 10^{20} atoms/cm^3 at 0.0 μm;

limitations from claim 26, the method of claim 21, in fig. 9, line 170; wherein the region includes a top surface, and a layer of carbon formed at the top surface, 10^{20} atoms/cm^3 at 0.0 μm;

limitations from claim 27, the method of claim 26 wherein the region includes silicon and germanium, p. 3, ¶ 37;

Chu gives motivation in p. 1, ¶ 3. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Chu's process with Banerjee's invention would have been beneficial because Chu reduces contaminates.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Banerjee as applied to claims 10-19, 21, 22, 24, 25, 28, 29 above, and further in view of Kubo et al., US Patent No. 6,399,970 B2.

Banerjee does not state using two differently doped semiconductor wells, but Kubo does. Kubo teaches in fig. 1, a well region of one conductivity type 11 with layer of silicon, germanium, and carbon, 15n and a well second type 12, col. 8, line 38 - col. 9, line 50. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Kubo's process with Banerjee's invention would have been beneficial because different polarity transistors increases circuit design flexibility.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Brewster

17 August 2005
WB